WE CLAIM:

1. A method of scheduling dispatch of packets containing constant bit rate (CBR) or real time variable bit rate (rt-VBR) at an ingress operation of multiplexing the packets into payloads of an asynchronous transfer mode (ATM) bearer virtual circuit connection, the method comprising controlling the packet dispatch so as to match the traffic characteristics of an underlying bearer channel.

2. A method as claimed in claim 1, wherein packets are dispatched according to two or more levels of packet priority.

3. A method as claimed in claim 2, wherein said packets are ATM Adaptation Layer Two (AAL2) packets.

4. A method of scheduling dispatch of packets containing constant bit rate (CBR) or real time variable bit rate (rt-VBR) at an ingress operation of multiplexing the packets into payloads of an asynchronous transfer mode (ATM) bearer virtual circuit connection, the method comprising;
enabling a holdover timer having a pre-set period on receipt of a packet;
assembling common part sublayer payload data unit (CPS-PDU) comprising any unused octets from a previous packet partially dispatched, and whole packets in order of priority;
whenever said timer period expires before a said common part sublayer payload data unit is completed, packing the payload of that data unit with null data; and
controlling the packet dispatch so as to match the traffic characteristics of an underlying bearer channel.

5. A method as claimed in claim 4, wherein said packets are stored in respective queues according to two or more priority levels, and wherein packets are preferentially taken from that queue having the higher or highest priority level.

6. A method as claimed in claim 5, wherein a partially completed common part sublayer payload data unit containing packets from said higher or highest priority queue is completed with one or packets from a lower priority queue.

7. A method as claimed in claim 6, wherein scheduling of completed cells is determined from a sustained cell rate and a peak cell rate for the virtual circuit connection.

8. A method as claimed in claim 7, wherein said packets are ATM Adaptation Layer Two (AAL2) packets

9. A packet scheduler for dispatch of packets containing constant bit rate (CBR) or real time variable bit rate (rt-VBR) at an ingress operation of multiplexing the packets into payloads of an asynchronous transfer mode (ATM) bearer virtual circuit connection, the scheduler comprising;
a holdover timer having a pre-set period on receipt of a packet;
assembly means for assembling common part sublayer payload data unit (CPS-PDU) comprising any unused octets from a previous packet partially dispatched, and whole packets in order of priority and, whenever said timer period expires before a said common part sublayer payload data unit is completed, for packing the payload of that data unit with null data; and
means for controlling the packet dispatch so as to match the traffic characteristics of an underlying bearer channel.

10. A packet scheduler as claimed in claim 9, wherein said packets are stored in respective queues according to two or more priority levels, and wherein packets are preferentially taken from that queue having the higher or highest priority level.

11. A packet scheduler as claimed in claim 10, and arranged to complete a partially completed common part sublayer payload data unit, containing packets from said higher or highest priority queue, with one or packets from a lower priority queue.

12. A packet scheduler as claimed in claim 11. wherein scheduling of completed cells is determined from a sustained cell rate and a peak cell rate for the virtual circuit connection.

13. A packet scheduler as claimed in claim 12, wherein event timing is effected via event timer ring buffers and an event store by associating event data in an event store location with a corresponding location in an event timer ring buffer.

14. A packet scheduler as claimed in claim 13, and in the form of an integrated circuit.